

High-Quality Large-Area Graphene for Device Applications

Timothy J. Lyon,^{1, a)} Jonas Sichau,¹ August Dorn,¹ Amaia Zurutuza,² Amaia Pesquera,² Alba Centeno,^{2, b)} and Robert H. Blick^{1, c)}

¹⁾ Center for Hybrid Nanostructures (CHyN), Department of Physics, University of Hamburg, Jungiusstrasse 9-11, 20355 Hamburg, Germany

²⁾ Graphenea, Avenida de Tolosa 76, 20018 Donostia-San Sebastian, Spain

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We describe a method for transferring ultra large-scale CVD-grown graphene sheets. These samples can be fabricated as large as several cm^2 and are characterized by magneto-transport measurements on SiO_2 substrates. The process we have developed is highly effective and limits damage to the graphene all the way through metal liftoff, as shown in carrier mobility measurements and the observation of the quantum Hall effect. The charge-neutral point is shown to move drastically to near-zero gate voltage after a 2-step post-fabrication annealing process, which also allows for greatly diminished hysteresis.

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Graphene is well-known for its desirable electrical properties,¹ and with all of the intense focus on research in the material, new applications are being constantly discovered. While graphene is known to have its best electrical properties when it is single-crystalline and suspended,^{2,3} those attributes are currently not feasible for mass-produced devices. There have been very exciting developments related to improving non-suspended graphene's mobility on more exotic substrates such as hBN,^{4,5} as well as improving the chemical vapor deposition (CVD) growth process for producing better quality devices with large grain sizes.⁵⁻⁷ However, these developments are currently difficult to scale up and automate.

On the other hand, CVD-grown graphene is still the best way to repeatably produce large areas of monolayer graphene, and SiO_2 is a well-known substrate that is already integrated into many processes from semiconductor physics to MEMS,^{8,9} and beyond. Previous work has shown how to transfer large areas of CVD-grown graphene onto arbitrary substrates¹⁰⁻¹³ and remove contaminants.^{10,14} However, previous CVD-grown graphene on SiO_2 devices do not combine the desirable properties of high enough quality electrical characteristics to display the quantum Hall effect (QHE), a charge neutral point (CNP) near zero gate voltage, and a large device size, with typical finished devices being on the order of $10\text{ }\mu\text{m}$.¹⁵ Large-scale integration of easily manufactured, high-quality graphene devices is desirable in many different applications, such as graphene transistors, broadband optical modulators¹⁶ and THz antennas.¹⁷

Challenges arise when fabricating high-quality CVD-grown graphene devices, primarily due to contaminants of all kinds easily attaching to graphene. With each step, much care must be taken to remove any existing organic

or inorganic contaminants on the graphene as well as prevent new contaminants from being attached. This paper presents a fabrication method that produces devices with CVD-grown graphene on SiO_2 that are hundreds of microns in size and display the QHE.

A sheet of copper is supplied with CVD-grown graphene on only one side. Other sources of CVD graphene on copper typically have graphene on both sides of the foil, and in that case an oxygen plasma can be used to remove graphene from one side. A wet transfer process is used to place the graphene on the substrate, with cleaning steps to remove inorganic and organic contaminants from the bottom of the graphene before transfer. These steps are similar to the method detailed by Liang *et al.*, which itself includes a “modified RCA clean” process.¹⁰

It is important to be sure that all contaminants from the graphene are removed, as any resist residues can act as dopants and scattering centers to degrade electrical performance^{2,3} as well as increase contact resistance.^{18,19} Acetone or other common solvents are not sufficient to remove residues from resists such as poly(methyl methacrylate) (PMMA). A common technique to clean small graphene devices is to use current annealing,²⁰ especially when the graphene is suspended, as it can effectively evaporate many contaminants and allow the graphene to self-heal.²¹ Other cleaning methods include mechanical cleaning with atomic force microscopy,²² exposure to ultra-violet light,²³ ozone treatment,^{18,23} and annealing in vacuum²⁴ or with gas flow.²⁵ In the process detailed in this paper, the graphene is cleaned before transfer to a clean substrate, and then cleaned again after fabrication by a 2-step thermal annealing process.

The size of the graphene/copper foil pieces used here is $1\text{ cm} \times 1\text{ cm}$, however, the process can easily be upscaled to sizes of several cm^2 . PMMA with a molecular weight of 950K is spun onto the graphene/copper foil and dried by air (Fig. 1(a)). A solution of $\text{Fe}(\text{NO}_3)_3$ is prepared with 5 g/100 ml of DI water and the PMMA/graphene/copper stack is placed to float in the solution with the copper side down, then left for at least 10 hours for the cop-

^{a)}Electronic mail: tlyon@wisc.edu; Also at Department of Physics, University of Wisconsin-Madison, 1150 University Ave, Madison, Wisconsin 53706, USA.

^{b)}<http://www.graphenea.com>

^{c)}<http://www.nanomachines.com>

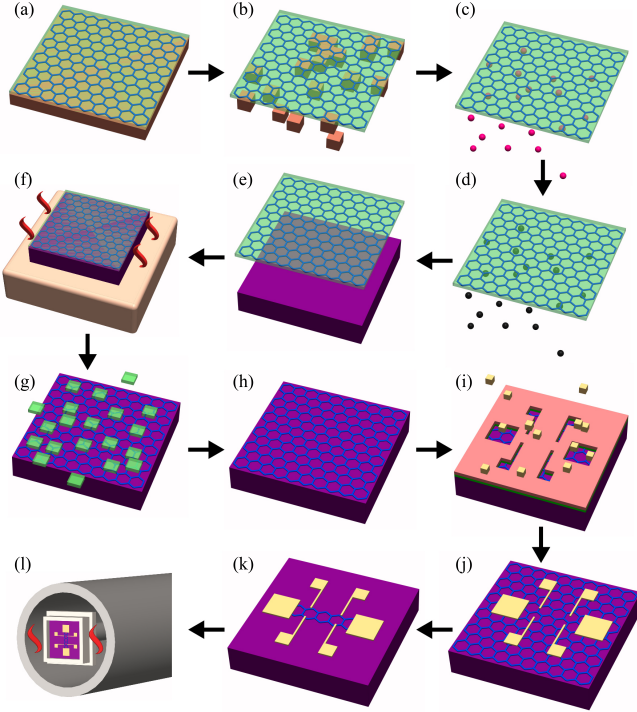


FIG. 1. Flow diagram of the sample preparation. PMMA is spun onto the graphene copper stack (a), before the copper is etched away (b). The graphene is cleaned in multiple steps removing inorganic (c) and organic (d) contaminants, scooped up with a SiO₂ wafer piece (e) and then dried (f). The PMMA layer is removed with acetic acid (g) and the result is shown in (h). For the definition of the Hall contacts, the sample is coated with layers of LOR and photoresist, exposed and developed, before Ni and Au are deposited as adhesion and contact materials, respectively (i). After lift-off (j), the excess graphene is etched away (k) and the sample is mounted in a probe and baked under vacuum (l).

per to etch away (Fig. 1(b)). Subsequently, the graphene stack is transferred to clean DI water at least twice, waiting 5 minutes after each transfer. Similarly to Liang *et al.*, the RCA clean step referred to as Standard Clean 2 is next, with a HCl/H₂O₂/H₂O solution prepared in a 1:1:20 ratio. Once again, the stack is placed on this solution to clean inorganic contaminants not removed by the Fe(NO₃)₃, such as oxides, for 15 minutes (Fig. 1(c)). The stack is then once again transferred to clean beakers of DI water at least twice for 5 minutes each. Finally, the RCA clean step known as Standard Clean 1 (SC-1) is performed with a NH₄OH/H₂O₂/H₂O solution in a 1:1:100 ratio for 5 minutes (Fig. 1(d)) to remove organic contaminants. The cleaning time and chemical concentrations of H₂O₂ and NH₄OH in SC-1 are lower than reported in the modified RCA clean process in order to avoid bubble formation. Bubbles that get under the graphene stack can lead to the graphene tearing and are very difficult to remove before transfer. After the SC-1 step is complete, the graphene is again transferred to clean beakers of DI-water twice, waiting 5 minutes after each transfer.

Wafers of thermally grown SiO₂ on *p*-doped Si are pre-

pared by carefully cutting into appropriately sized pieces with a diamond scribe. Any contaminants are cleaned off with sonication in acetone and then isopropanol before the wafers are dried with a N₂ gun. The SiO₂ is then treated with O₂ plasma in order to make the surface more hydrophilic²⁶, so the graphene will stick to it more readily and minimize breakage. Within one minute of the substrate's O₂ plasma exposure, the PMMA/graphene stack is scooped up and it is all dried in an oven set to 150 °C for 15 minutes (Fig. 1(e) and (f)). Finally, the PMMA is removed with acetic acid (Fig. 1(g)), which more cleanly removes PMMA residue than acetone, while at the same time not attacking either the graphene or the SiO₂ substrate.¹⁴ At this point, the graphene is cleanly transferred to the substrate with minimal cracks or tears (Fig. 1(h)), with most defects existing previous to the transfer process. Many other defects can be explained by bumps, folds, or other surface features in the copper foil that the graphene was grown on. These features make it much less likely for the graphene to transfer tear-free, making it very important to keep the copper foil as flat as possible. As shown in Fig. 2(a) and 2(b), Raman spectra at 532 nm were taken in multiple locations to verify reproducibility of the measurement and uniformity of the graphene monolayer.

Once the graphene is on the target substrate, it must still have metal contacts deposited as well as be patterned into whatever shape is desired. Both of these steps must ideally be done without damaging or contaminating the graphene any more than absolutely necessary. The contacts are defined using photolithography, with a layer of Microchem LOR 5A used between the photoresist and graphene. This bi-layer stack tends to remove much more cleanly than photoresist alone²⁷ and after removal can result in high-quality devices. In our observation, it also results in a higher final yield of usable devices due to less undesired graphene removal during liftoff. Without a protective layer of LOR, negative photoresists tended to result in much worse yield than positive resists, possibly due to crosslinking of polymer chains during exposure. After exposure and development, a 5 nm layer of Ni is deposited by physical vapor deposition as an adhesion layer, followed by 50 nm of Au (Fig. 1(i)). Liftoff is then performed in a two-phase process. First, the sample is soaked in a bath of acetone, which removes the photoresist and lifts off the excess metal. Since an ultrasonic bath will damage the graphene, excess metal is instead gently removed by squeezing a pipette to agitate the acetone. Second, after all excess metal is removed, the LOR layer is removed by being soaked in Microposit Remover 1165 for five minutes. Finally, the sample is rinsed with isopropanol and dried with a N₂ gun. The result is shown in Fig. 1(j).

For this sample, excess graphene is removed by using photolithography to cover the areas of graphene to be protected from O₂ plasma. The sample is then chemically cleaned for the final time with acetone and isopropanol, then dried with N₂. Fig. 1(k) and 2(c) show the final

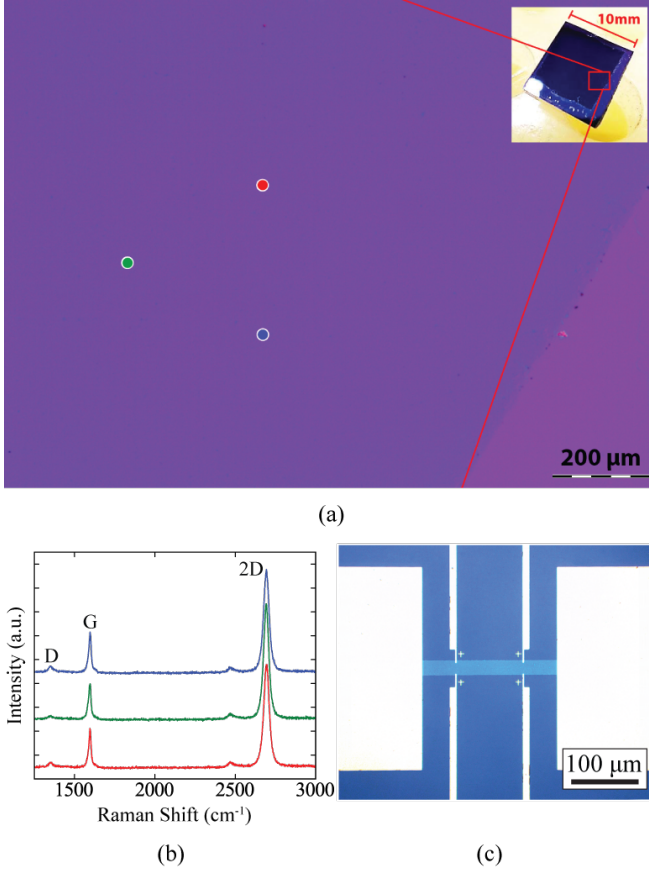


FIG. 2. (a) Optical microscopy image of a large clean area of graphene (dark purple) on a SiO_2 substrate (light purple). Inset: Picture of a $1\text{ cm} \times 1\text{ cm}$ SiO_2 wafer with CVD graphene on top (dark blue). (b) Raman spectra with a 532 nm laser taken at the colored spots shown in (a), displayed with an artificial offset for clarity. The defect peak D is very small in all three measurements, which speaks for a high quality of graphene. Also, due to the relative height of the G and 2D peaks, which is about one third, we can confirm that we see a monolayer of graphene.²⁸ (c) Optical microscopy image of a $200\text{ }\mu\text{m}$ long and $22\text{ }\mu\text{m}$ wide graphene strip (light blue) on an SiO_2 substrate (dark blue) with a contact layout typical for Hall measurements. (Graphene contrast increased for visual effect in (a) and (c)).

result.

The sample is then mounted in a probe with air pumped out and replaced with a small quantity of He as an exchange gas. The longitudinal resistance is measured over a range of applied gate voltages at a temperature of 4.2 K at zero magnetic field. The sample is annealed under vacuum for 16 hours at 350°C to remove all water, including water trapped between the graphene and substrate. The sample is then removed from vacuum and quickly mounted in a probe, and once again annealed in a tube oven under vacuum (Fig. 1(i)) at 140°C for 72 hours to remove any water absorbed from the atmosphere during mounting. During this time, the 2-point resistance of the Hall bar is observed to steadily increase from approximately $25\text{ k}\Omega$ to a new maximum of $57\text{ k}\Omega$. Fig. 3 shows the increase in peak longitudinal resistance

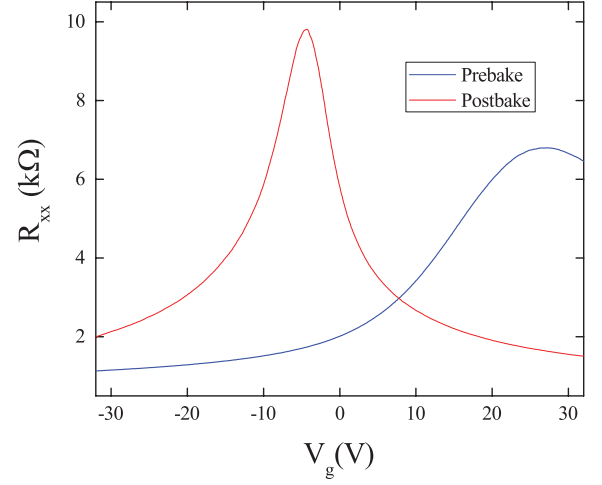


FIG. 3. Longitudinal resistance R_{xx} of the graphene strip versus gate voltage V_g before (blue) and after (red) baking out the sample. The measurements were recorded at $T = 4.2\text{ K}$. A possible explanation for the postbake shift of the CNP of over 30 V is the removal of contaminants on the graphene that act as dopants, originating from resist residues or the atmosphere.

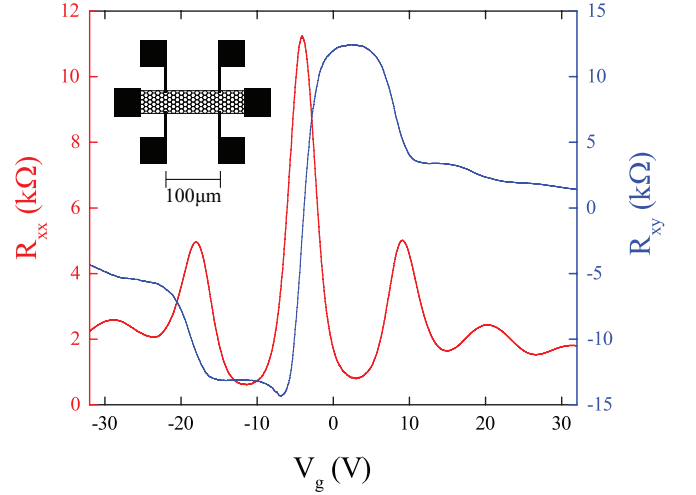


FIG. 4. The longitudinal (red) and Hall resistance (blue) versus the gate voltage V_g at fixed magnetic field $B = 8\text{ T}$ measured at 4.2 K , obtained through a standard 4-point-measurement approach, show multiple quantum Hall levels. Inset: Schematic of the graphene strip and contacts, with a distance between the longitudinal contacts of $100\text{ }\mu\text{m}$.

along with a dramatic shift of the charge neutral point (CNP) from $V_g = 27\text{ V}$ to -4 V before and after annealing, respectively, which is evidential of the concentration of charged impurities being significantly reduced.²⁹ The large peak shift is indicative of the removal of a majority of p -type dopants such as water³⁰ and the settling of the CNP at a negative gate voltage may be due to doping by the metal contacts or contact doping by SiO_2 and any contaminants trapped between the graphene and metal during processing.^{31,32}

The CNP changes by at most 0.1 V , depending on the

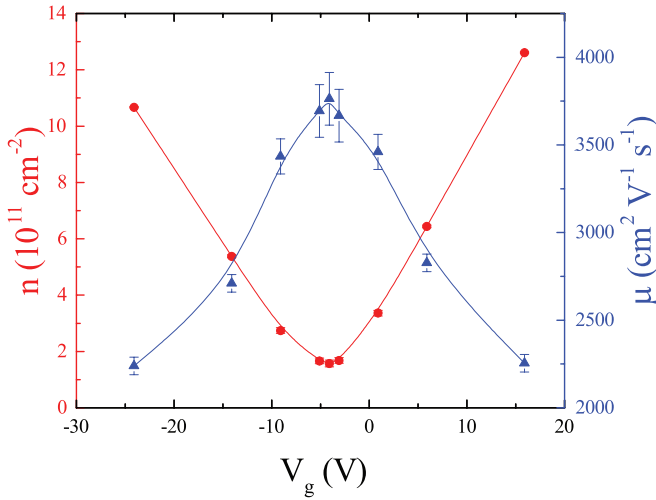


FIG. 5. The charge carrier density (red) and mobility (blue) versus the gate voltage V_g at 4.2 K after the final annealing step. The values were obtained by performing magnetoresistance measurements at the displayed values for V_g . Points are connected by B-spline curves. The charge carrier density is linear with respect to gate voltage away from the CNP, which implies the gate oxide provides the dominant capacitive effect which is expected due to the oxide thickness.³⁴ The rounding of the charge carrier density graph near the CNP is due to charged electron/hole puddles induced by charged impurities, including those in the substrate.²⁹

direction the gate voltage is swept. When there is still a significant amount of water on the substrate, this hysteresis can easily be on the order of a few or even tens of volts.²⁶ This effect is typical of graphene on SiO_2 and the relatively low hysteresis seen in this sample implies that most of the water has been removed by the previous annealing step.³³

The magnetic field is then set to 8 T and the gate voltage is scanned once more at 4.2 K. Multiple quantum Hall levels were seen, as shown in Fig. 4. Clear plateaux for the Hall resistance, R_{xy} , at filling factors of $\nu = \pm 4(n + 1/2)$ and Landau level index $n = 0, 1, \dots$ are seen with corresponding drops in the longitudinal resistance, R_{xx} .³⁵ Further magnetoresistance measurements were performed to find charge carrier density and mobility at nine different gate voltages with the result shown in Fig. 5. At the CNP, the mobility is measured to be around $\mu_{\text{CNP}} = 3760 \text{ cm}^2/(\text{Vs})$ and the charge carrier density is $n_{\text{CNP}} = 1.58 \times 10^{11} \text{ cm}^{-2}$. These measurements show that the fabrication method presented here results in a mobility at the charge neutral point that approaches values obtained when using exfoliated graphene on SiO_2 ,³⁶ implying that the graphene is very clean and has been minimally damaged by the sample production process.

In summary, we have presented a procedure that results in clean large-area graphene devices of high quality on a SiO_2 substrate. The 2-step liftoff aids greatly in unbroken large graphene structures, and the 2-step annealing process as well as other cleaning steps result in a realization of near-ideal mobilities and a low hysteresis

with observation of quantum Hall levels. This process is thus suited for large-scale integration of high quality graphene devices.

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